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A Review of Resistor Switching Devices for Memory and Neuromorphic Computing Applications

Research Article

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Abstract

High-density memories are required for various applications in the area of signal and image processing, Digital system design, and neural networks. Researchers are looking for an intermediate solution to fill the gap between DRAM and Flash NAND in the memory hierarchy. The development of Resistive Switching Technologies (RRAM) proposes a potential solution to this demand for fast, low cost, high density, and non-volatile memory. This paper discusses the schematic of Resistive Switching (RS) devices, The Principle and operation of memristor crossbar array as memory, potential applications of memristors as memory, Logic design applications, and neuromorphic computations.

Introduction

Over the past decades, successive downscaling of the complementary metal-oxide-semiconductor (CMOS) transistors consistent with Moore's law has contributed to the exponential progress in computing and knowledge technology. The amount of transistors per microprocessor chip has doubled about every two years with increased clock speed or rate of execution of instructions. The transistor size is approaching the elemental physical limit of around 2–3 nm beyond which quantum tunneling and quantum uncertainties will make transistors unreliable to work in conventional circuits. Additionally, the performance gap between processing and memory units has increased dramatically, and therefore the data movement between these units within the conventional Von-Neumann architecture starts to be the foremost dominant factor for energy consumption and system throughput [4, 5]. This problem, widely referred to as the Von-Neumann bottleneck, is going to be further exacerbated within the data-intensive applications like machine learning tasks. to deal with these issues, new materials, devices, and new computing architectures are now extensively investigated to enrich and possibly replace conventional CMOS devices and circuits. One such device may be a non-volatile Resistive Switching (RS) device. rather than using electrons and holes to store data in conventional memory units, RS devices store data by reconfiguring the interior ion (oxygen ion or metal cation) distribution in nanoscale solid-state films.

A typical RS device stores data in the form of different values of resistance, and has a simple two-terminal resistor-like structure with a functional thin film sandwiched by two electrodes, as schematically shown in Figure. 1. RS devices first received broad interest as they effectively reduce the performance gap between existing memory (i.e. static random-access memory (SRAM) and dynamic random-access memory (DRAM)) and non-volatile data storage solutions, and can potentially replace the above memoriesdue to the fast switching speed, low power operation, scalability and good reliability offered by RS devices [1].

Memristor Theory

Memristor characteristics and Relationships

Passive circuit theory can be described asa set of relationships between electromagnetic quantities:

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1) Voltage vis the change inmagnetic flux Φ for time *t*
2) Current iis the change in electric charge *q* for time *t*
3) Resistor Ris a linear relationship between voltage and current (*dv* = *Rdi*)
4) Capacitor Cis the linear relationship between voltage and electric charge (*dq* = *Cdv*)
5) Inductor Lis the linear relationship between magnetic flux Φ and current i (dΦ = Ldi)

Out of the six possible relationships, the sole two electromagnetic quantities that there are not any pairings are magnetic flux and charge. But, in 1971 Leon Chua [6] postulated that mathematically, a fourth fundamental passive circuit element could exist, called a memristor, that binds the charge q to the linkage flux Φ as shown in Figure. 2 during which the electrical symbol of a memristor is additionally indicated:

dΦ = Mdq ----- (1)

The memristoris defined in terms of a non-linear functional relationship between the flux linkage Φ(t) and the amount of electric charge that has flowed through the device q(t):

f(*Φ*(*t*),*q*(*t*)) = 0 ---- (2)

where *Φ*(*t*) and q(t)are time-domain integrals of memristor electric voltage *v* and electric current *i*, respectively:

$$\Phi(t) = \int_{-\infty}^{t} v(\tau)d\tau \quad \text{----- (3)}$$

and

$$q(t) = \int_{-\infty}^{t} i(\tau)d\tau \quad \text{----- (4)}$$

The variable flux linkage Φ(t) is borrowed from the circuit characteristic of an inductor, and it does not represent a magnetic field here.In Eq. (2) the derivative of one respect to the other depends on the value of one or the other. The charge-dependent rate of change of flux with chargecan be used to describe the memristor function as:

$$M(q) = \frac{d\phi}{dt} \quad \text{------ (5)}$$

Introducing Eq, (3) in Eq, (5), we have:

$$M(q(t)) = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = R_M(q) \quad \text{------ (6)}$$

where $R_M(q)$ is the small-signal memristancedefined at the operating point. In this way, we have acharge-controlled or current-controlled memristor. Similarly, simplifying Eq, (4) in (5), we have:

$$M(\phi(t)) = \frac{\frac{dq}{dt}}{\frac{d\phi}{dt}} = G_M(\phi) \quad \text{------ (7)}$$

In this way, we will obtain a flux-controlled or voltage-controlled memristor. The current-controlled memristor is often modelled as a classical resistor whose resistance is controlled by the time-domain integral of the present flowing through the memristor. Analogously, the voltage-controlled memristor behaves as a conductor whose conductance depends on the time domain integral of terminal voltage.

In both cases, need an electronically controlled resistor,conductor and an integrator. Table.1 covers all meaningful ratios of differentials of i, q, Φ, and v. Figure. 3 shows the current-voltage characteristics for memristor, with its pinched hysteresis loop [2].

With reference to Eq. (6), memristor function can also be written in the following way;

Figure 1. Schematic of two-terminal RS device.

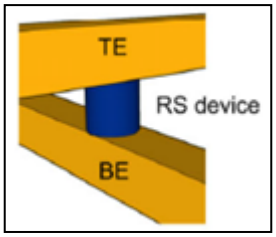


Figure 2. Memristor Relationship.

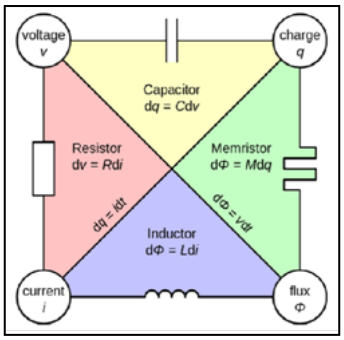
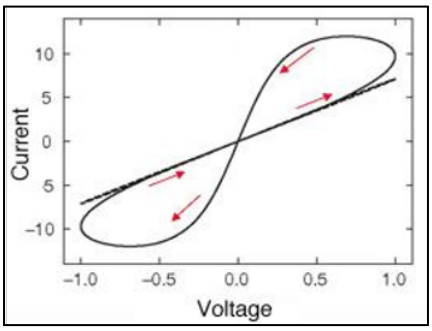


Table 1. Ratios of differentials of *i, q, Φ,* and *v.*

Device	Units	Differential Equation
Resistor	Ohm	R=dv/di
Capacitor	Farad	C= dq/dv
Inductor	Henry	L= dΦ/di
Memristor	Ohm	M= dΦ/dq

Figure 3. Current - Voltage characteristics of Memristor.



$v(t) = M(q(t))\, i(t)$ ----- (8)

The power consumption characteristic equation of a memristor is given by,

$P(t) = V(t)\, I(t) = I^2(t) M(q(t))$ ----- (9)

As long as M(q(t)) varies little, such as under alternating current, the memristor will appear as aconstant resistor.When *M(q(t))* increases rapidly, the current and power consumption will quickly stop.

Memristor Read and Write operation

The memristor stores the logical value in terms of its resistance, in contrast to standard memories, which use a charge to represent data. This resistance is controlled by applying a voltage across the memristor. Memristors are often fabricated between two metals, which act as the top and the bottom electrodes of a switching dielectric material. Hence, memristors are often fabricated within the metal layers as a part of a typical CMOS Back End of Line (BEOL) process. Memristive memory generally utilizes a crossbar structure, which enables a particularly dense memory array with a memory cell area of 4F2, where F is the technology feature size. Figure.4 shows one such design of a memristive memory crossbar array. Voltage drivers, row/column decoders, and sense amplifiers are used as a component of the peripheral circuit to support write and read operations, similar to other memory technologies.

To perform a write operation, a write voltage Vwrite, above the threshold voltage (Von and Voff, which switches the memristor to LRS and HRS, respectively), is applied across the target memristor through the wordlines and bitlines. For a memristor with asymmetric switching characteristics (i.e.,Von = Voff), two different write voltages are applied for writing logic 1 (i.e., VSET) and 0 (i.e., VRESET). Read operations are performed by applying a voltage Vread , with a magnitude less than the threshold voltage for switching, and measuring current passing through the device employing a sense amplifier [3].

Resistive Switching Memory Device Applications

Memory applications

RS devices are considered as one of the simplest applicants for future non-volatile memory applications [7, 8]. Unlike charge-based memories, like dynamic random access memory (DRAM) and NAND non-volatile storage, which affect performance degradation as the scaling limit is approached, non-charge based memories including RS devices offer solutions to increase Moore's law. especially, ionic RS devices offer outstanding performance specs including scalability, high switching speed, long retention time, high endurance, large on/off ratio, and low power operation. Memory applications uses the resistance states of RS devices represent a touch ('0' or '1') or multi bits (e.g. 2bits: '00', '01', '10', or '11'), which may be read by sensing current through the RS device during the read operation.

In-memory computing: Deep learning accelerator

Synaptic functions: In addition to memory applications, RS devices are considered promising candidates for bio-inspired computing and in-memory computing. When applied in computing systems, the RS devices are often utilized in a crossbar form to perform Vector matrix operation (VMM). During this approach, the values within the matrix are stored as the analog conductance values of the RS devices within the crossbar array. The input vector is applied as voltage pulses with different pulse amplitudes or different pulse widths to the rows of the crossbar. The currents or charges collected at the columns of the crossbar represent the resulting VMM outputs. As a result, the compute-intensive VMM operations are often obtained during a single step, greatly improving the energy efficiency and throughput beyond the restrictions of standard computing.In the nervous system, a neuron can communicate with other neurons by passing electrical or chemical signals through synapses [9]. Each neuron is often connected with thousands of other neurons with different connection strength, i.e. synaptic weight, which determines how efficient the input spikes from one neuron (the

Figure 4. Crossbar structure of Memristive memory array.

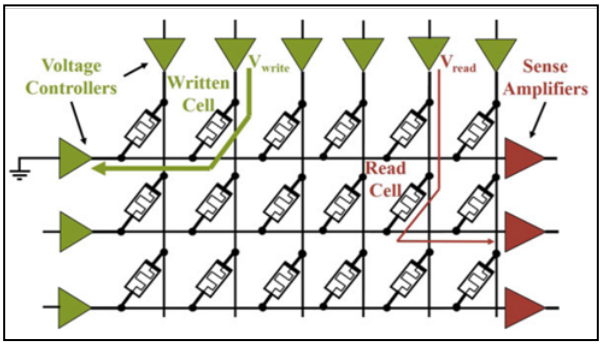
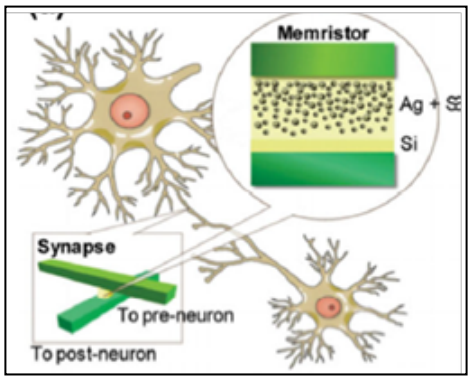


Figure 5. Schematic of the concept of RS devices as synapses between neurons.



pre-synaptic neuron) are often delivered to the receiving neuron (the postsynaptic neuron). Additionally, the synaptic weight are generally updated by spikes from the pre- and post-neurons, allowing the system to achieve learning and form memory. These structures and functions are implemented with RS device networks, thus making it possible to realize highly-efficient bio-inspired computing hardware.

VMM with crossbar array: In deep learning algorithms, the VMM operation (Multiply-Accumulate (MAC) operation) is the main computing operation for training and inference but is extremely resource expensive for conventional computing systems to implement. To accelerate VMM efficiently, the graphics processing unit has been extensively used to improve parallelism by using 1,000 s of computing cores with a high-throughput connection to the memory. Algorithm studies to more efficiently map the neural networks (NNs) onto the hardware have also been conducted [10]. New hardware "accelerators", like the tensor processing unit (TPU), was also designed to enhance the efficiency of matrix operations and have benefited the success through optimizations of the digital circuit and architecture design for these relatively narrow types of operations [11]. Unlike conventional hardware systems, RS crossbar array structures can naturally perform VMM during a single read step [12]. The Neural Network structure is readily mapped to the crossbar arrays, where the RS devices located at each cross point can store the weight matrix values also as producing an output depending on the input and therefore the weight. The inputs and outputs of the network (or a layer within the network) are connected to rows and columns of the crossbar array, respectively as shown in Figure 6. During inference, read voltage pulses are fed to the rows of the crossbar particular to the input signals, the VMM outputs are collected as the current through the crossbar array at the columns as shown in Figure 6. The VMM operation is completed concurrently with none of the data movement between processing and memory unitsirrespective of the matrix size, thus offering very high parallelism that results in superior computing throughput and very high energy efficiency [13, 14].

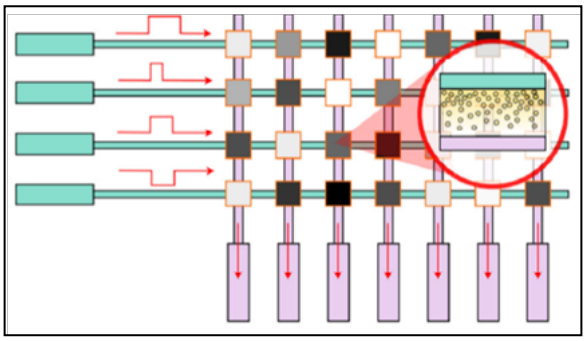
Logic design applications

RS devices have also been used for logic operations in electronic circuits, which offers a high compute density and non-volatility. A fundamental Boolean logic operation, material implication (IMP), isimplemented as a logic gate two RS devices. Logic values can be represented by the resistance of the RS devices (i.e., "0" for the High resistance State-HRS and "1" for the Low resistance state-LRSand the IMP operation can be achieved based on the voltage divider effect. With well-designed voltage pulses and series resistance values, the resistance of the output RS device (q) is determined by the input logic state (p), producing the desired truth table for the IMP operation. With iterative IMP operations, all other Boolean logic operations can then be achieved [15, 16]. Beyond logic applications, RS devices are often used as non-volatile switches in field-programmable gate arrays (FPGA) systems [17-19]. Switches using RS devices are reprogrammed to reconfigure the connections and therefore the functionality of the FPGA, resulting in improved density and power metrics. RS devices can act as logic elements that summarise the data paths connecting logic gates into digital circuits, enabling FPGA-like functionality.

Conclusions

In this paper, we have highlighted the history, operation of RS devices as a memory for reading and write operation and its potential applications. RS devices have made remarkable progress over the last 15 years. RS devices have offered

Figure 6. A RS device for VMM for on a crossbar.



commercial productsfor memory applications and have also been extensively used for neuromorphic computing applications, providing significant benefits for real-time data processing with highthroughput and low energy consumption.

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